Claims

We claim:

1. A lateral IGFET device comprising:

a semiconductor substrate having a first conductivity type;

a region of semiconductor material comprising alternating layers of first and second conductivity type material deposited over the semiconductor substrate and having a first major surface;

a drain region of the second conductivity type extending from the first major surface into at least a portion of the region semiconductor material;

a body region of the first conductivity type formed in a portion of the region of semiconductor material and extending partially from the first major surface into the region of semiconductor material;

a first source region formed in the body region; and

a trench gate structure formed in a portion of the region of semiconductor material, wherein the trench gate structure controls a sub-surface channel region.

2. The device of claim 1 wherein in the drain region comprises a trench filled with a doped polycrystalline material.

3. The device of claim 1 wherein the trench gate structure is filled with a doped polycrystalline material of the second conductivity type, and wherein the trench gate structure extends from the first major surface adjacent the source region and a portion of the body region into the region of semiconductor material, and wherein the trench

gate includes a first gate dielectric layer formed at least on sidewall surfaces of the trench gate structure.

4. The device of claim 3 further comprising a first doped region of the second conductivity type formed adjacent a portion of the sidewall surfaces.

5. The device of claim 1 further comprising a surface gate structure formed over the first major surface, wherein the surface gate structure controls conduction in a surface channel region.

6. The device of claim 1 wherein a lower portion of the trench gate structure terminates within the semiconductor substrate.

7. The device of claim 1 wherein one layer of the alternating layers adjacent the first major surface comprises the first conductivity type.

8. The device of claim 7 wherein the one layer is thicker than adjacent layers in the region of semiconductor material.

9. The device of claim 1 further comprising a first doped region of the second conductivity type formed in the region of semiconductor material adjacent the first major surface and between the body region and the drain region.

10. A lateral MOSFET device comprising:

a semiconductor substrate;

a region of semiconductor material including a plurality of alternating layers of first and second conductivity semiconductor material formed over the semiconductor substrate and having a major surface;

a trench drain structure formed in the region of semiconductor material;

a trench gate structure formed in the region of semiconductor material;

a body region of first conductivity type formed adjacent the trench gate structure; and

a source region of the second conductivity type formed in the region of first conductivity type.

11. The lateral MOSFET device of claim 10 further comprising a surface gate portion formed over the major surface adjacent the trench gate structure and the source region.

12. The lateral MOSFET device of claim 10 further comprising a doped region of the second conductivity type formed in the region of semiconductor material adjacent a portion of the trench gate structure.

13. The lateral MOSFET device of claim 10 wherein the region of semiconductor material includes a layer of the first conductivity type at the major surface, and wherein the layer has a thickness greater than adjacent layers within the region of semiconductor material.

14. The lateral MOSFET device of claim 10 wherein at least a portion of the alternating layers within the region of

semiconductor material extend between the trench drain structure and the trench gate structure.

15. The lateral MOSFET device of claim 10 wherein the trench drain structure includes a trench filled with a polycrystalline semiconductor material having the second conductivity type.

16. The lateral MOSFET device of claim 10 wherein the trench gate structure extends further into the region of semiconductor material than the trench drain structure.

17. An insulated gate FET structure comprising

alternating layers of first and second conductivity type material forming a semiconductor region;

a trench gate structure formed in the alternating layers, wherein the trench gate structure controls a sub-surface channel region;

a drain region of the second conductivity spaced apart from the trench gate structure and extending into the alternating layers; and

a source region of the second conductivity type formed adjacent to the trench gate structure.

18. The insulated gate FET structure of claim 17 wherein the drain region comprises a trench filled with a polycrystalline semiconductor material.

19. The insulated gate FET structure of claim 18 wherein the trench gate structure extends into the alternating layers deeper than the drain region.

20. The insulated gate FET structure of claim 17 wherein the trench gate structure controls a plurality of sub-surface channel regions.